24.7 A Low-Jitter and Precise Multiphase Delay-Locked Loop Using Shifted Averaging VCDL

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For the DLLs and PLLs with multiphase outputs, the timing accuracies of the multiphase clocks will depend on the matching among delay stages. However, the mismatch among active devices with short lengths worsens for advanced sub-micron technologies. The mismatch-induced error voltage in the differential delay stages leads to unbalanced currents or capacitances to affect the absolute accuracy of the delay stages. The delay of this particular stage is longer or shorter than the normal one. One of the solutions to reduce the mismatch is to increase the transistor size. However, the chip area and parasitic capacitances increase. Another solution is to dynamically calibrate the mismatch [1,2]. It may not only increase chip area but also noise. The proposed DLL using the shifted-averaging VCDL can average the mismatch of the differential delay stages. It provides the equal delay time and the enhanced duty cycle for the inner stages without extra hardware required.

Figure 24.7.1 shows all the phases for a VCDL with ten differential delay stages in a DLL. Of interest is that *clk*(*i*)+ and *clk*(*i*)- are in phase with *clk*(*i*+5)- and *clk*(*i*+5)+, respectively. The *clk*(*i*)+ is the positive output of the *i*th stage, *clk*(*i*)- is the negative output of the *i*th stage, and $0 \le i \le 5$. Figure 24.7.2 shows the proposed shifted averaging VCDL. For instance, *clk*5+ could substitute the input signal of the first stage, *ref*-, while *ref*- could substitute the input signal of the sixth stage, *clk*5+. Since the inputs of each delay stage do not come from the same stage, the mismatch-induced errors occurred at the outputs of the differential delay stages is independent and mutually uncorrelated. Most important is that the shifted averaging technique changes only the interconnection of the differential delay stages and does not increase the hardware and power dissipation of the VCDL.

The proposed shifted averaging VCDL has two features. First, this VCDL can average the timing errors of the delay stages. Assume that the nominal delay time for a delay stage is T_d. Suppose that there are a positive timing error, Δt_1, at the positive output (clk1+) and a negative one, $-\Delta t_1$, at the negative output (clk1-) in the first delay stage of Fig. 24.7.2. This results in the duty cycle of the conventional delay stages to be larger or smaller than the normal value, 50%. Consider the shifted-averaging VCDL in Fig. 24.7.4, where the total delay time from ref+ to clk10- can be expressed as

$$t_{total}=15 \bullet T_d+\Delta t_1-\Delta t_1=15 \bullet T_d \qquad (1)$$

Moreover, the total delay time from *ref*- to clk10+ is $5T_d$. The timing errors have been averaged to enhance the duty cycle and reduce the static timing error. The same method can be applied to the timing error for other delay stages. The proposed shifted averaging VCDL can strengthen the phase-to-phase relation of the inner stages and guarantees the 180^0 phase difference between the *jth* and the $j+\frac{N}{2}$th stages for $j=1 \sim \frac{N}{2}$ for N is even.

Second, the 3dB improvement in the jitter performance could be obtained by the shifted averaging technique. If a mismatch current error exists in the differential pair, an error voltage, Δv_n, is generated at the positive output and an opposite error voltage, $-\Delta v_n$, is generated at the negative output. The delay time for a delay stage can be expressed as [3]

$$T_d+\Delta\tau \approx (V_{SW}+\Delta v_n) \times \frac{C_L}{I_{tail}} \qquad (2)$$

where Δv_n is the random error voltage, $\Delta\tau$ is random timing error, V_{SW} is the voltage swing of the delay cell, T_d is the delay time of a delay stage, C_L is the output loading capacitance of a delay stage, and I_{tail} is the tail current. If the inputs of the delay stages come from the outputs of different delay stages and their random error voltages are independent, the random timing error would be reduced by a factor of $\sqrt{2}$ as shown in the following.

$$\bar{\Delta\tau}=E(\Delta\tau_m+\Delta\tau_n)=\frac{\tau}{\sqrt{2}} \qquad m \neq n \qquad (3)$$

In addition, this technique does not increase chip area and power dissipation.

The proposed DLL shown in Fig. 24.7.3 is composed of a phase detector (PD), a charge pump circuit (CP), the lock detector (LD) which provides a pumping current to reduce the lock time in the initialization state, the differential-to-single-ended (DTS) converter, the loop filter, and the shifted averaging VCDL in Fig. 24.7. 2.

Both the conventional DLL and the shifted-averaging DLL have been fabricated in a CMOS 0.35μm 1P 4M process and the whole chip area is 1.5x1.5mm^2 including I/O pad peripherals. The die photo is shown in Fig. 24.7.4. Figure 24.7.5 shows the locked state of the conventional DLL and the proposed one, respectively, at 150MHz. From Fig. 24.7.5, the proposed DLL reduces the static phase error and enhances the duty cycle in the lock state. Fig. 24.7.6 shows the output jitter histograms of the conventional DLL and the proposed one, respectively, at an operating frequency of 150MHz. For the conventional DLL, the peak-to-peak jitter is 37.63ps, and rms jitter is 5.116ps. For the shifted averaging DLL, the peak-to-peak jitter is 26.38ps, and rms jitter is 3.411ps. Compared with a conventional DLL, the proposed one improves the peak-to-peak jitter by a factor of 1.4. Comparison of the skew errors and the peak-to-peak jitters of the conventional DLL and the proposed are displayed in Fig. 24.7.7. For the shifted averaging DLL, the peak-to-peak jitters of inner stages have the similar jitter distribution, but the peak-to-peak jitter of each stage is smaller. The skew errors of the shifted averaging DLL are reduced. Thus, the proposed DLL has better skew performance than the conventional one.

A low jitter and precise multiphase delay-locked loop using shifted averaging technique is proposed. Using the shifted averaging technique, the proposed DLL can reduce the mismatch-induced timing error among the delay cells without extra hardware required. It can not only generate precise multiphase outputs but also duty cycle enhancement. Experimental results also demonstrate the functionality of the proposed DLL which can reduce the skew errors and improve jitter performance of inner stages.

Acknowledgements

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References

[1] C. H. Park, O. Kim, and B. Kim, " A 1.8-GHz self-calibrated phase-locked loop with precise I/Q matching," *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 777-783, May 2001.

[2] L. Wu, W. C. B. Jr., "A low-jitter skew-calibrated multi-phase clock generator for time-interleaved applications," *ISSCC Dig. Tech. Papers*, pp. 396-399, 2001.

[3] G. Chien and P. R. Gray, "A 900-MHz local oscillator using a DLL-based frequency multiplier technique for PCS applications," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1996-1999, Dec. 2000

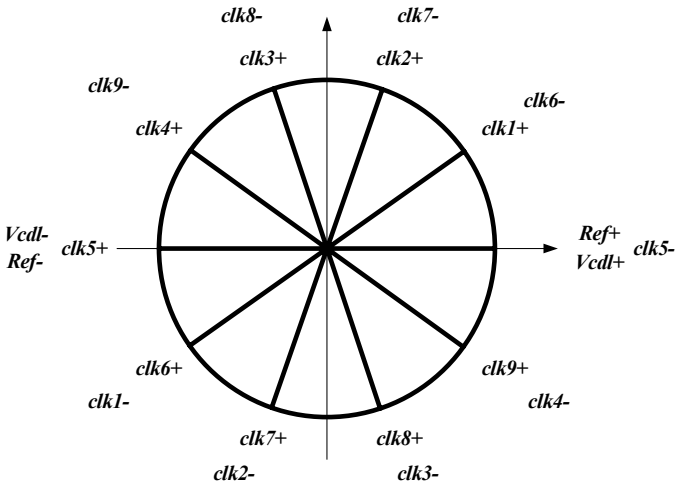


Figure 24.7.1: Phase diagram of N (=10) delay stages in the steady state.

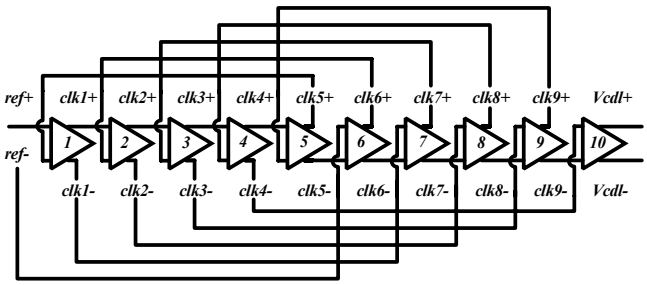


Figure 24.7.2: Shifted averaging VCDL.

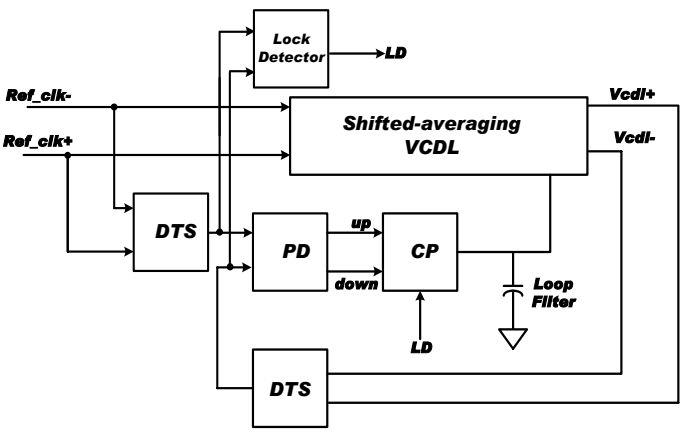


Figure 24.7.3: The proposed DLL.

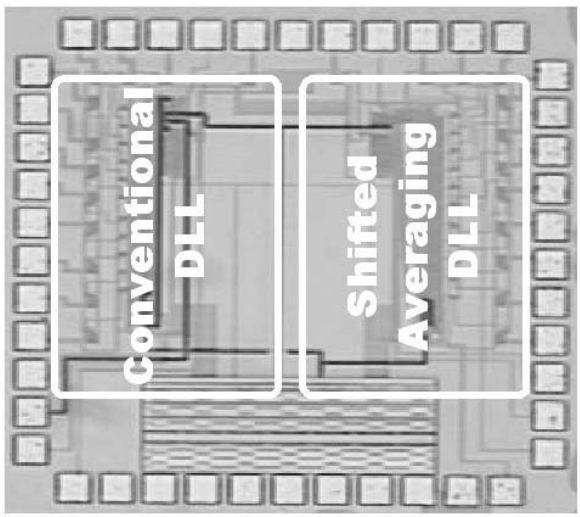
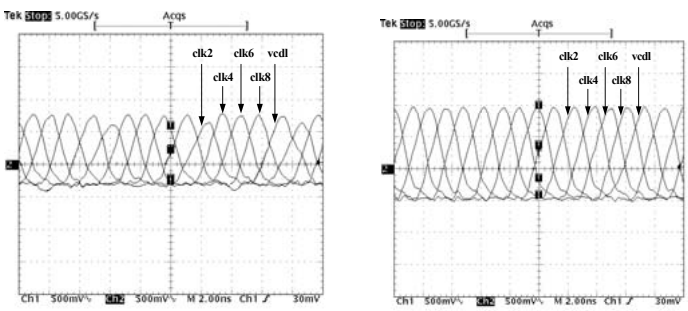


Figure 24.7.4: Die photo for two DLLs.



(a) Conventional DLL (b) Proposed DLL

Figure 24.7.5: Locked state at 150MHz.

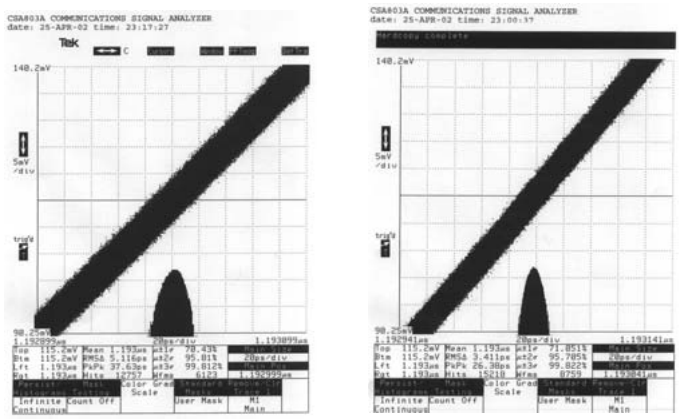


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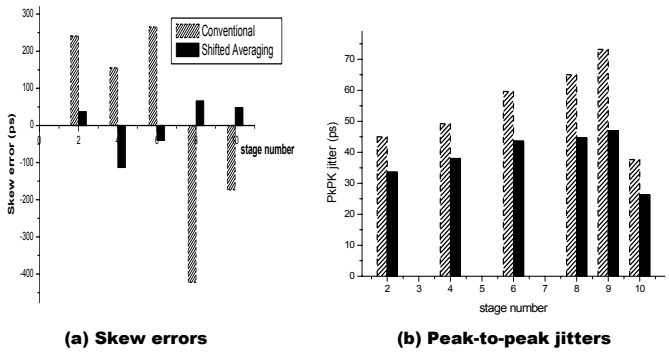
Figure 24.7.6: Jitter histogram at 150MHz.



(a) Skew errors **(b) Peak-to-peak jitters**

Figure 24.7.7: The measured skew errors and peak-to-peak jitters of VCDL inner stages.

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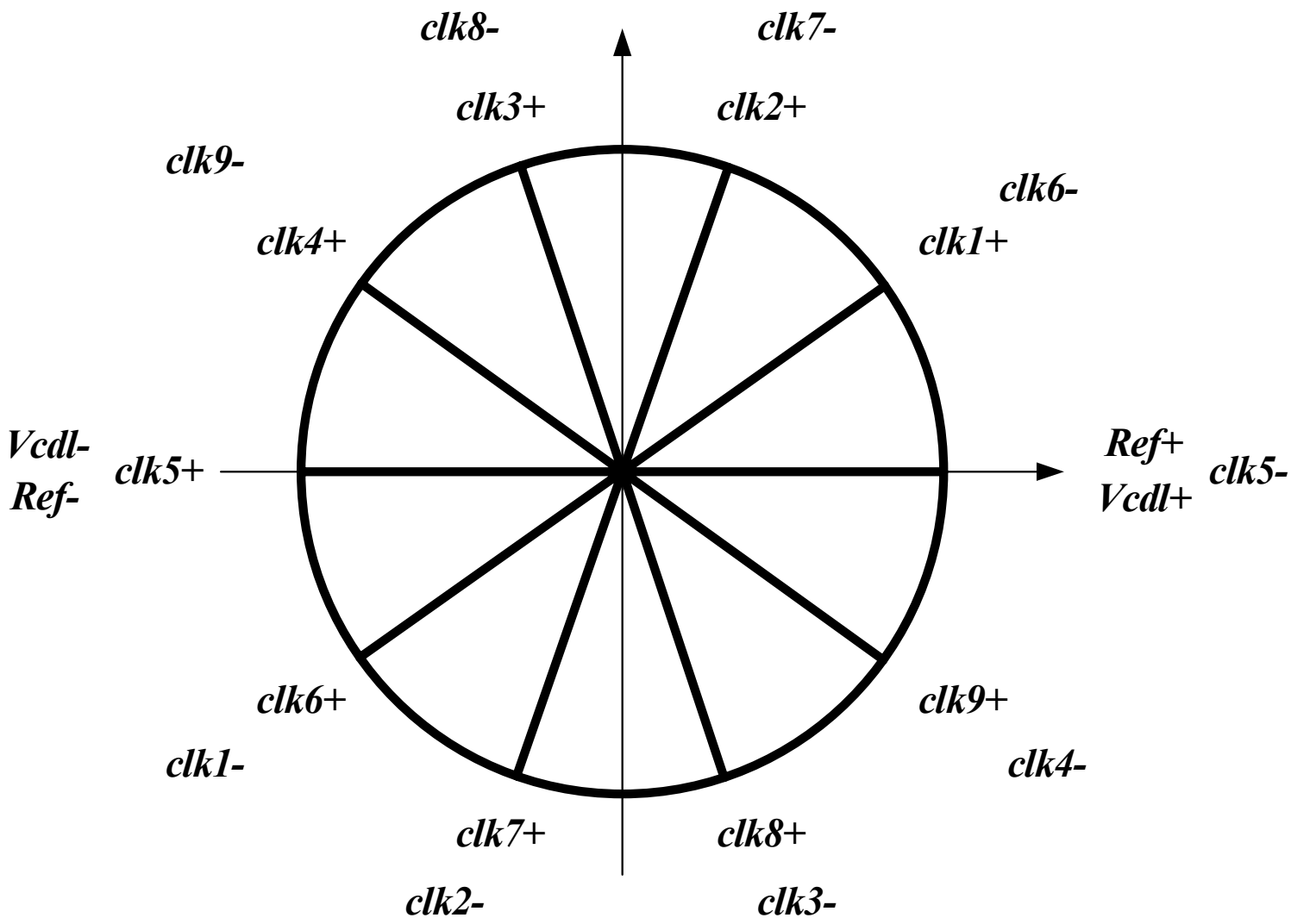

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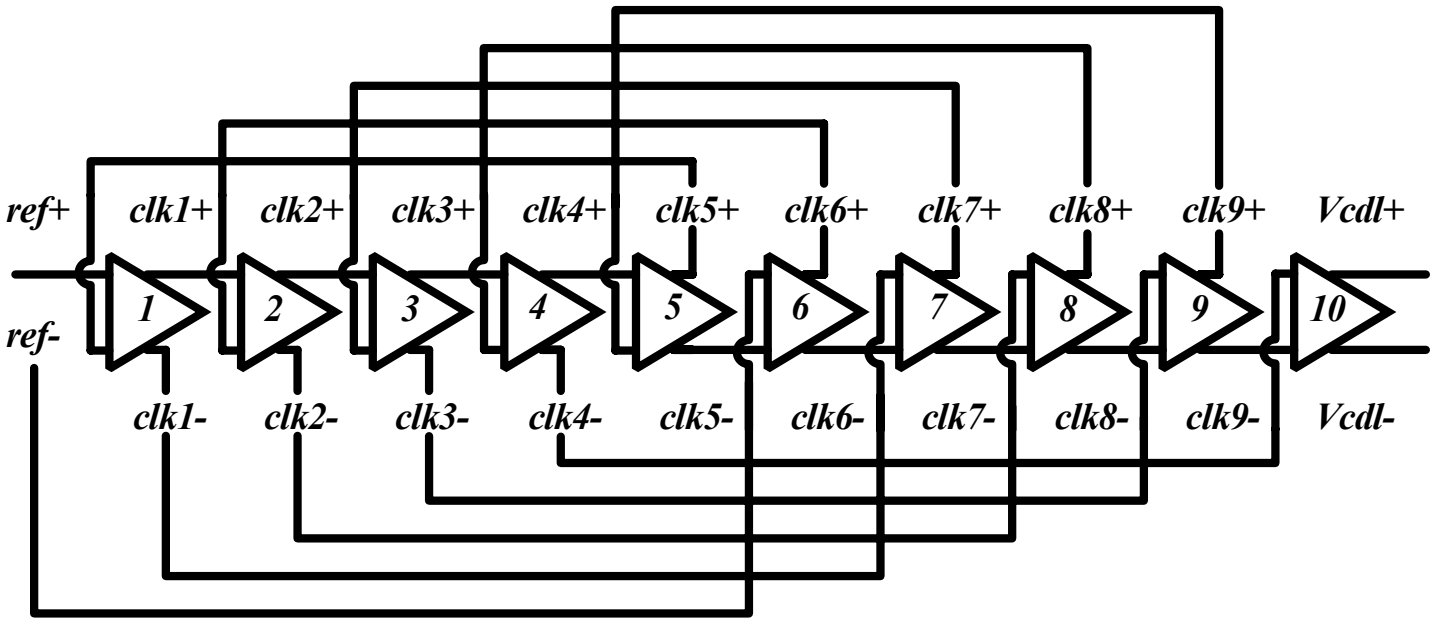

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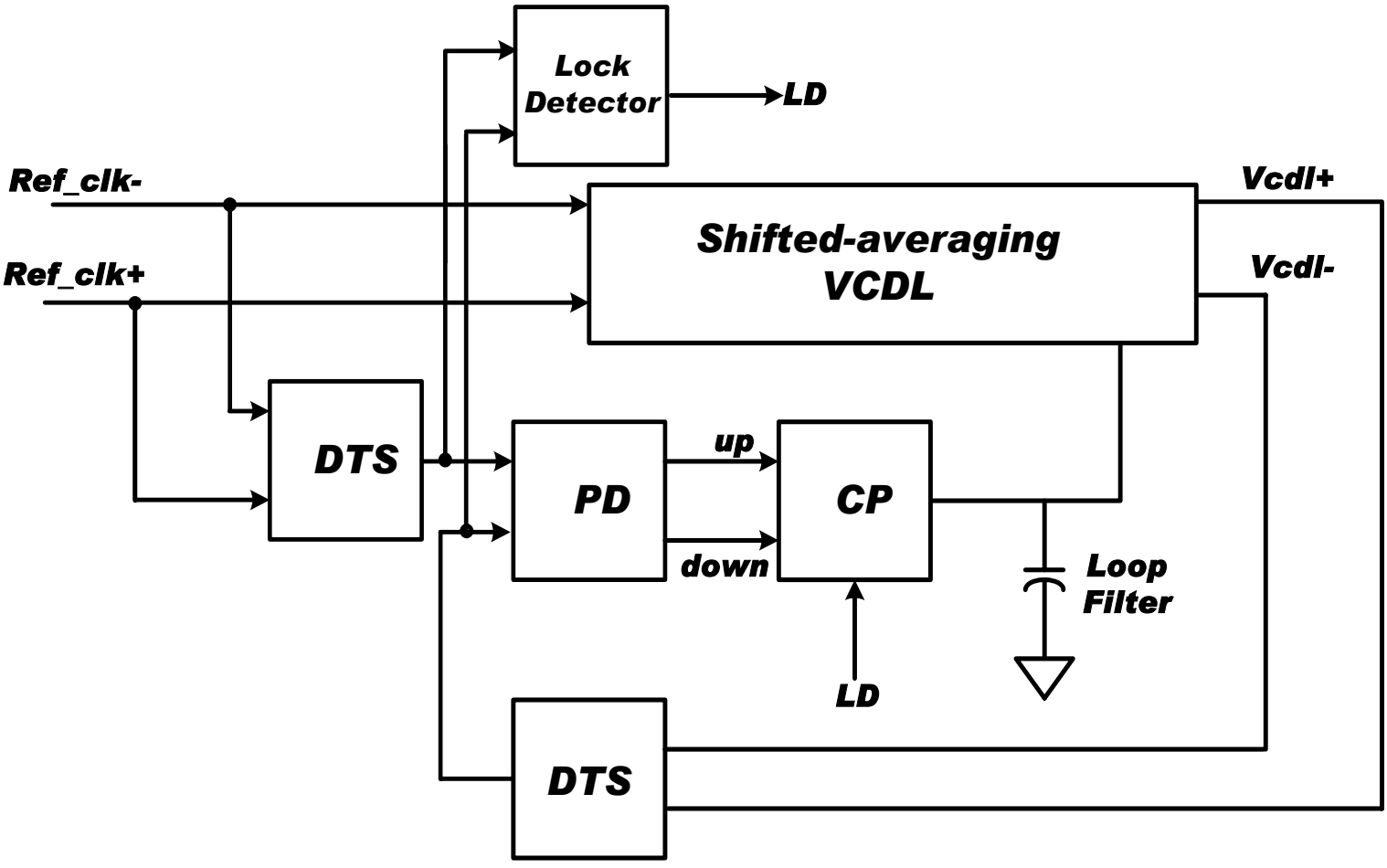

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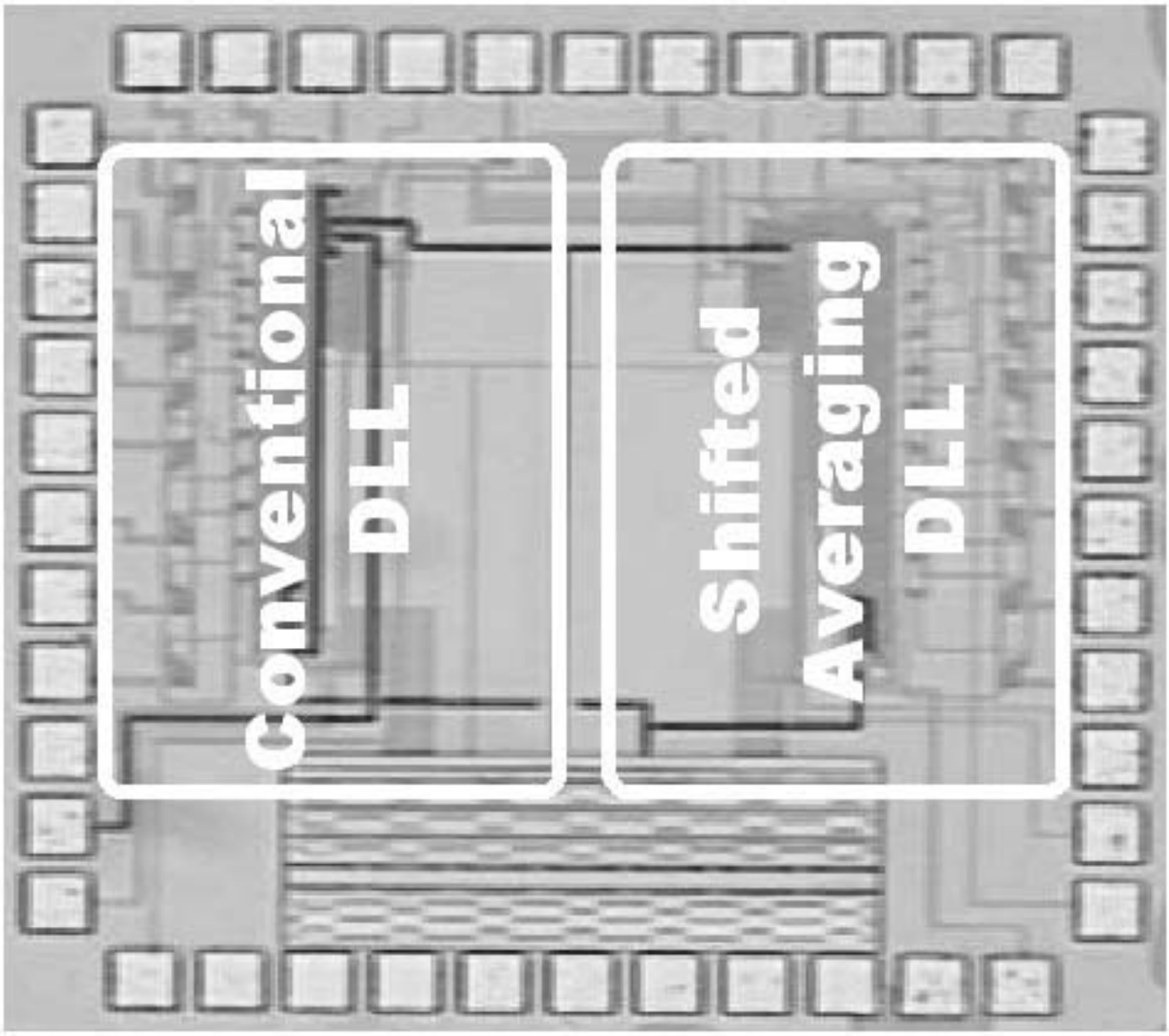
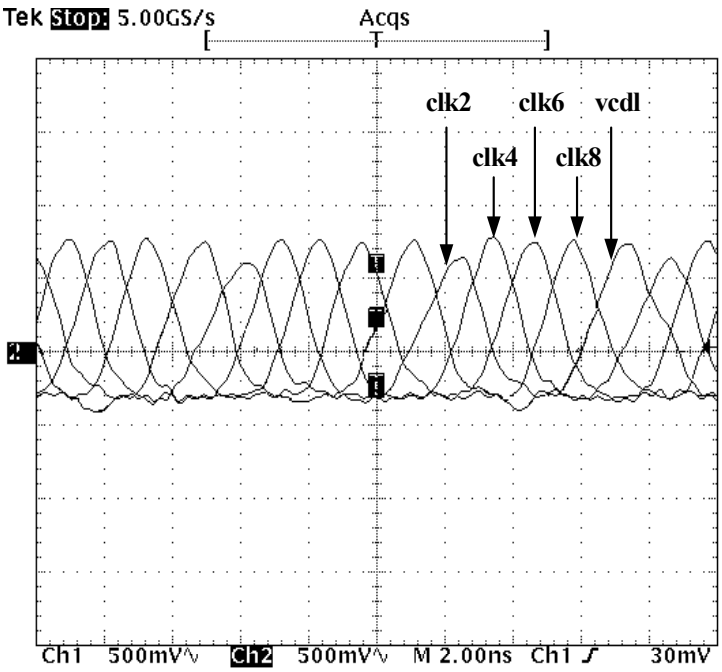
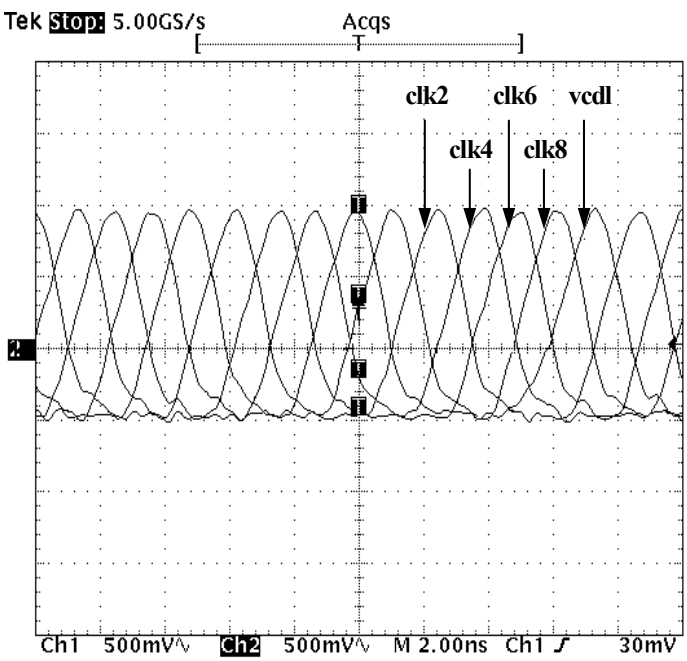


Figure 24.7.4: Die photo for two DLLs.



(a) Conventional DLL



(b) Proposed DLL

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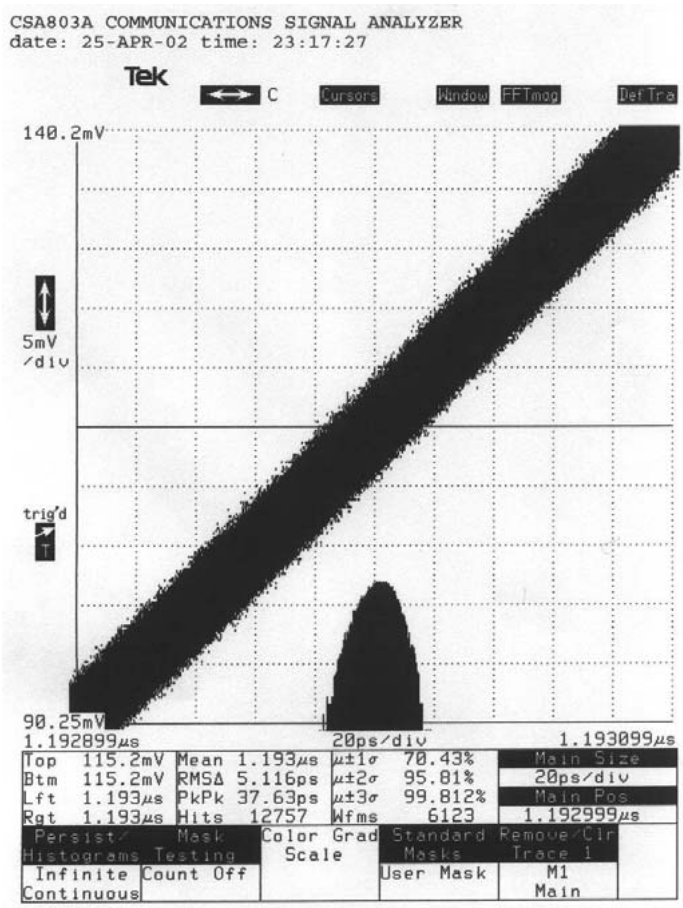

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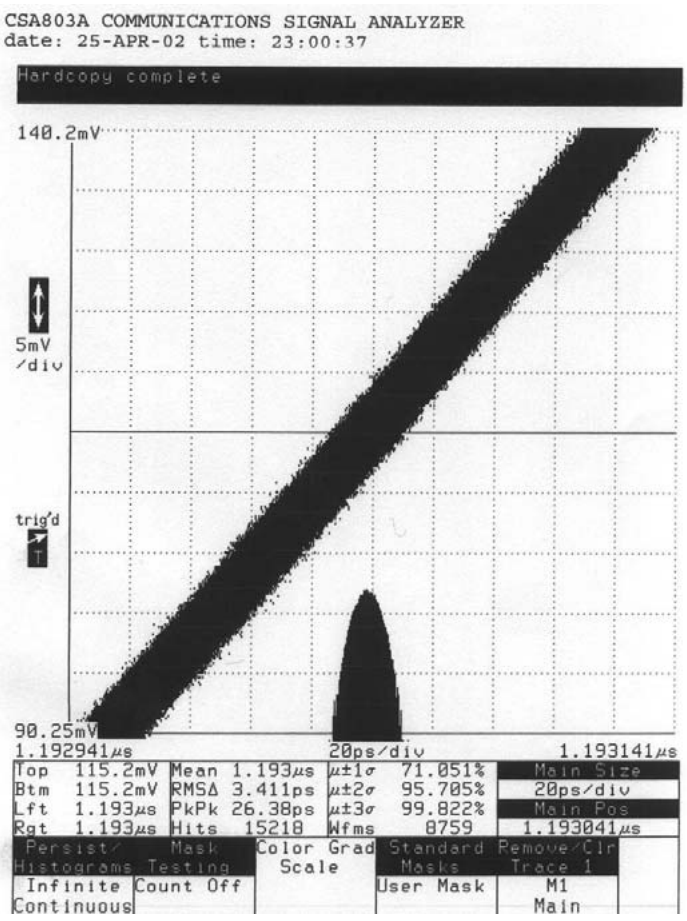
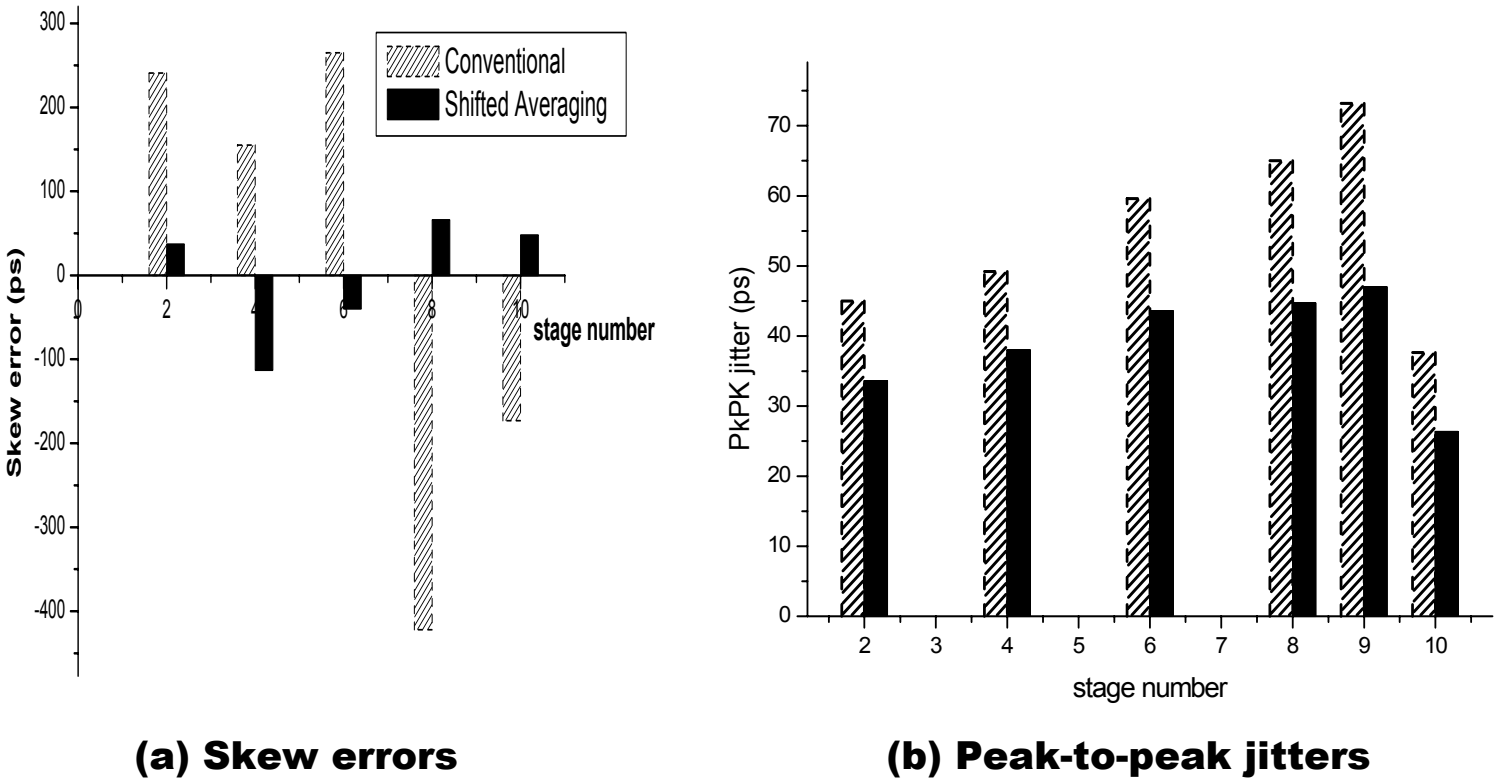


(b) Proposed DLL

Figure 24.7.6: Jitter histogram at 150MHz.



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